AN205

Composite Video Interfacing for the VP520S

Application Note

Supersedes February 1996 version, AN205 - 1.1

AN205 - 2.1 June 1996

The existing H.261 evaluation board for the GPS H.261 chipset requires video input from a Gen-locked RGB digital camera and outputs analog RGB and sync for display on an RGB monitor. This is an expensive solution and most people prefer to use a composite video input signal and display on a TV monitor. This application note is intended to provide a reference design for composite video input and output.

The solution used here is provided by four devices from Philips Semiconductors. For the video input three devices are required; TDA8708A, SAA7157 and SAA7151(Note: these three devices may be replaced in the future with the forthcoming Philips SAA7111 VIP Video Input Processor). To provide a CVBS output signal the SAA7188A is used.

The TDA8708A is an analog input interface for video signal processing. It includes a video amplifier with clamp and gain control, an 8-bit analog-to-digital converter (ADC) with a sampling rate of 32MHz and an input selector.

The SAA7157 Clock signal generator circuit (SCGC) generates all clock signals required for a digital TV system suitable for the SAA7151. The circuit operates in either the phase-locked loop mode (PLL) or voltage controlled oscillator mode (VCO).

The SAA7151 is a digital multistandard colour-decoder (DMSD2-SCART) having two 8-bit input channels, one for CVBS or Y, the other for chrominance or time-multiplexed colour-difference signals, it decodes digital TV signals with line-locked clock in PAL, SECAM and NTSC standards (CVBS or S-video) as well as RGB signals coming from a SCART/peri-TV connector.

8-bit CVBS data (digitized composite video) are fed to the SAA7151. The data rate is 27MHz.

The SAA7188A digital MPEG-compatible Video Encoder (DENC2-M) encodes digital luminance and chrominance into analog CVBS and simultaneously S-Video (Y/C) signals. NTSC-M and PAL B/G standards are supported.

The basic encoder function consists of subcarrier generation and color modulation as well as insertion of synchronization signals. Luminance and chrominance signals are filtered according to the standard requirements RS-170-A and CCIR-624.

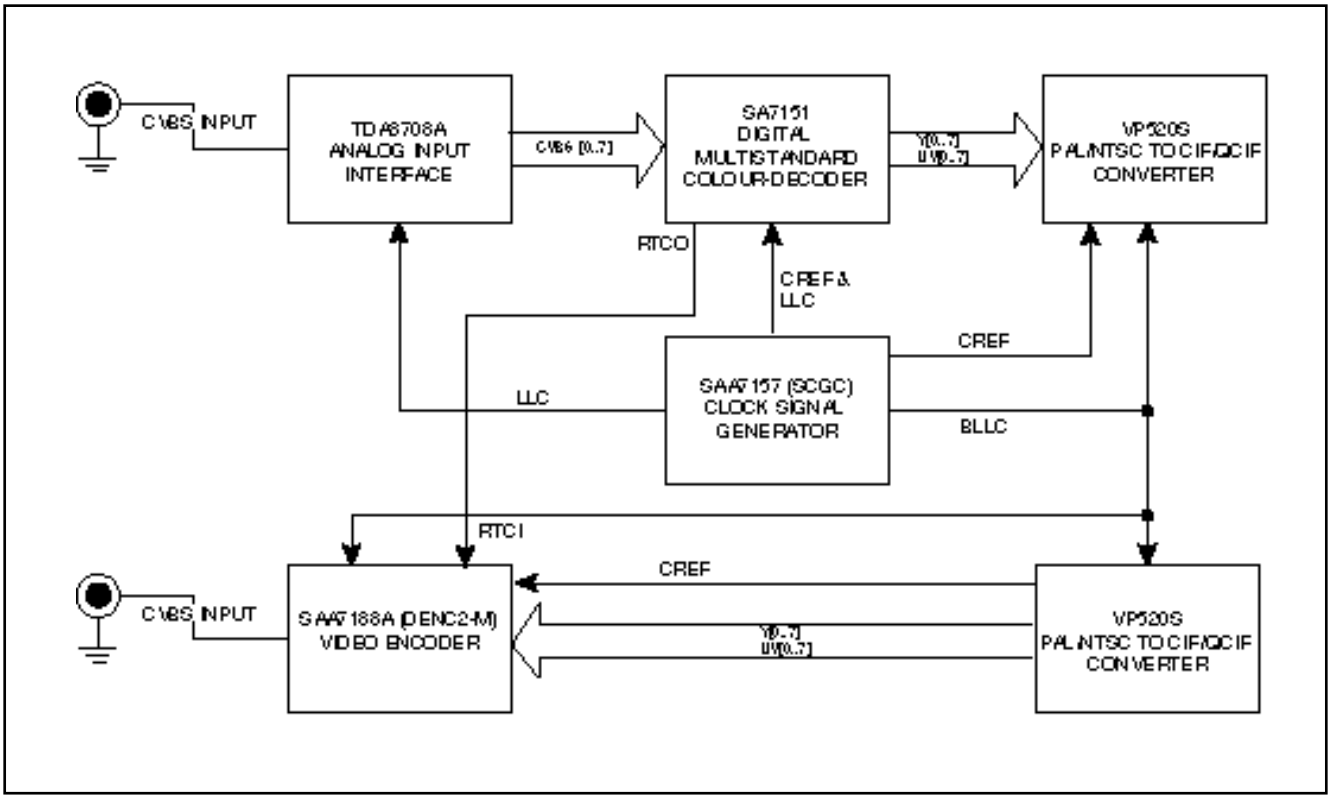

Fig.1 block diagram

COMPOSITE VIDEO INTERFACING FOR THE VP520S

SAA7151 PROGRAMMING DETAILS

Function	Subaddress	Data (Hex.)	Result
increment delay	00	64	64 increment delay - set up for generating LLC using DTO etc.
H-sync HSY begin	01	35	35 position of start of sync level synchonisation pulse for PAL
H-sync HSY stop	02	0A	position of start of sync level synchonisation pulse for PAL
H-clamp HSY begin	03	F8	position of start of black level synchonisation pulse for PAL
H-clamp HSY stop	04	CD	position of end of black level synchonisation pulse for PAL
H-sync after PHI1	05	FE	programmable hsync position - not used by H.261 design, Href indicates active video
luminance control	06	01	luminance control - CVBS input, no pre-emphasis, notch filter selected for PAL subcarrier
hue control	07	00	hue control - set to 0 degrees for PAL selected
control #1	08	1F	PAL for forced colour standard and colour killer threshold
control #2	09	1F	SECAM colour killer etc - irrelevant
PAL switch sensitivity	0A	90	PAL switch sensitivity
SECAM switch sensitivity	0B	90	SECAM switch sensitivity - irrelevant
control #3	0C	08	general purpose outputs (unused), chroma gain controlled by loop
control #4	0D	40	colour killer on, UV outputs straight binary, irrelevant SECAM bits
control #5	0E	B0	CCIR levels, colour on, syncs enabled, chroma from CVBS input
control #6	0F	90	auto field detect, 625 lines, PLL closed, TV mode
control #7	10	62	auto standard off, 4:2:2 format
chroma gain reference	11	4F	chroma gain
control #8	12	C0	enable YUV buses, normal vertical noise reduction

NOTE
1. These values are provided for reference and will need some adjustment for individual applications.
2. Refer to SAA7151 data sheet for detailed meaning of register settings.
3. Refer to Philips 1994 Desktop Video Data Handbook for details of I^2C timing details.

SAA7151 PROGRAMMING DETAILS

Function	Subaddress	Data (Hex.)	Result
NULL	00	00	
NULL	39	00	
Input_Port_Control	3A	0C	input_port_control, select straight binary YUV format
			OSD LUTs, CCIR 601 Colour Bars
OSD_LUT_Y0	42	6B	White
OSD_LUT_U0	43	00	White
OSD_LUT_V0	44	00	White
OSD_LUT_Y1	45	52	Yellow
OSD_LUT_U1	46	90	Yellow
OSD_LUT_V1	47	12	Yellow
OSD_LUT_Y2	48	2A	Cyan
OSD_LUT_U2	49	26	Cyan
OSD_LUT_V2	4A	90	Cyan
OSD_LUT_Y3	4B	11	Green
OSD_LUT_U3	4C	B6	Green
OSD_LUT_V3	4D	A2	Green
OSD_LUT_Y4	4E	EA	Magenta
OSD_LUT_U4	4F	4A	Magenta
OSD_LUT_V4	50	5E	Magenta
OSD_LUT_Y5	51	D1	Red
OSD_LUT_U5	52	DA	Red
OSD_LUT_V5	53	70	Red
OSD_LUT_Y6	54	A9	Blue
OSD_LUT_U6	55	70	Blue
OSD_LUT_V6	56	EE	Blue
OSD_LUT_Y7	57	90	Black
OSD_LUT_U7	58	00	Black
OSD_LUT_V7	59	00	Black
Chroma_Phase	5A	3F	phase of sc relative to h-sync
Gain_U	5B	7D	Gains set for White-Black = 100IRE
Gain_V	5C	AF	Gains set for White-Black = 100IRE
Gain_U_MSB, Black_lev	5D	2D	Gains set for White-Black = 100IRE
Gain_V_MSB, Black_lev	5E	3F	Gains set for White-Black = 100IRE
NULL	5F	00	Gains set for White-Black = 100IRE

NOTE
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COMPOSITE VIDEO INTERFACING FOR THE VP520S

SAA7151 PROGRAMMING DETAILS (cont'd)

Function	Subaddress	Data (Hex.)	Result
X-Col_Select	60	40	PAL cross colour filter on
Standard_Control	61	06	864 pixels per line, PAL encoding, No real-time control of sc
Burst_Amplitude	62	48	Amplitude of colour burst for PAL
Subcarrier_0	63	CB	Subcarrier frequency
Subcarrier_1	64	8A	set to PAL-B/G
Subcarrier_2	65	09	
Subcarrier_3	66	2A	
Line21_Even_0	67	67	Closed captioning not used
Line21_Even_1	68	68	Closed captioning not used
Line21_Odd_0	69	69	Closed captioning not used
Line21_Odd_1	6A	6A	Closed captioning not used
Encod_Crtl, CC_Line	6B	81	Closed captioning not used - encode inputs on VP port
RCV_Port_Control	6C	20	Syncs active hi, vref on RCV1, hblank on RCV2
RCM, CC-Mode	6D	00	Closed captioning & RCM outputs not used
H-Trigger	6E	0F	Can adjust output hsync referred to input with this
H-Trigger	6F	01	Can adjust output hsync referred to input with this
Fsc_Res_Mode, V-Trigger	70	80	reset subcarrier every eight fields for PAL
Begin_MP_Request	71	F9	RCM2, RCV2 outputs not used
End_MP_Request	72	86	RCM2, RCV2 outputs not used
MSBs_MP_Request	73	60	RCM2, RCV2 outputs not used
NULL	74	00	
NULL	75	00	
NULL	76	00	
Begin_RCV2_out	77	F9	RCM2, RCV2 outputs not used
End_RCV2_out	78	86	RCM2, RCV2 outputs not used
MSBs_RCV2_out	79	60	RCM2, RCV2 outputs not used
Field_Length	7A	70	length of field in half-lines (624 Lines)
First_Act_Line	7B	17	first active line after blank in lines (Line 23)
Last_Act_Line	7C	67	last active line before vertical blank (Line 615)
MSBs_Field_Ctrl	7D	22	msbs of above

NOTE
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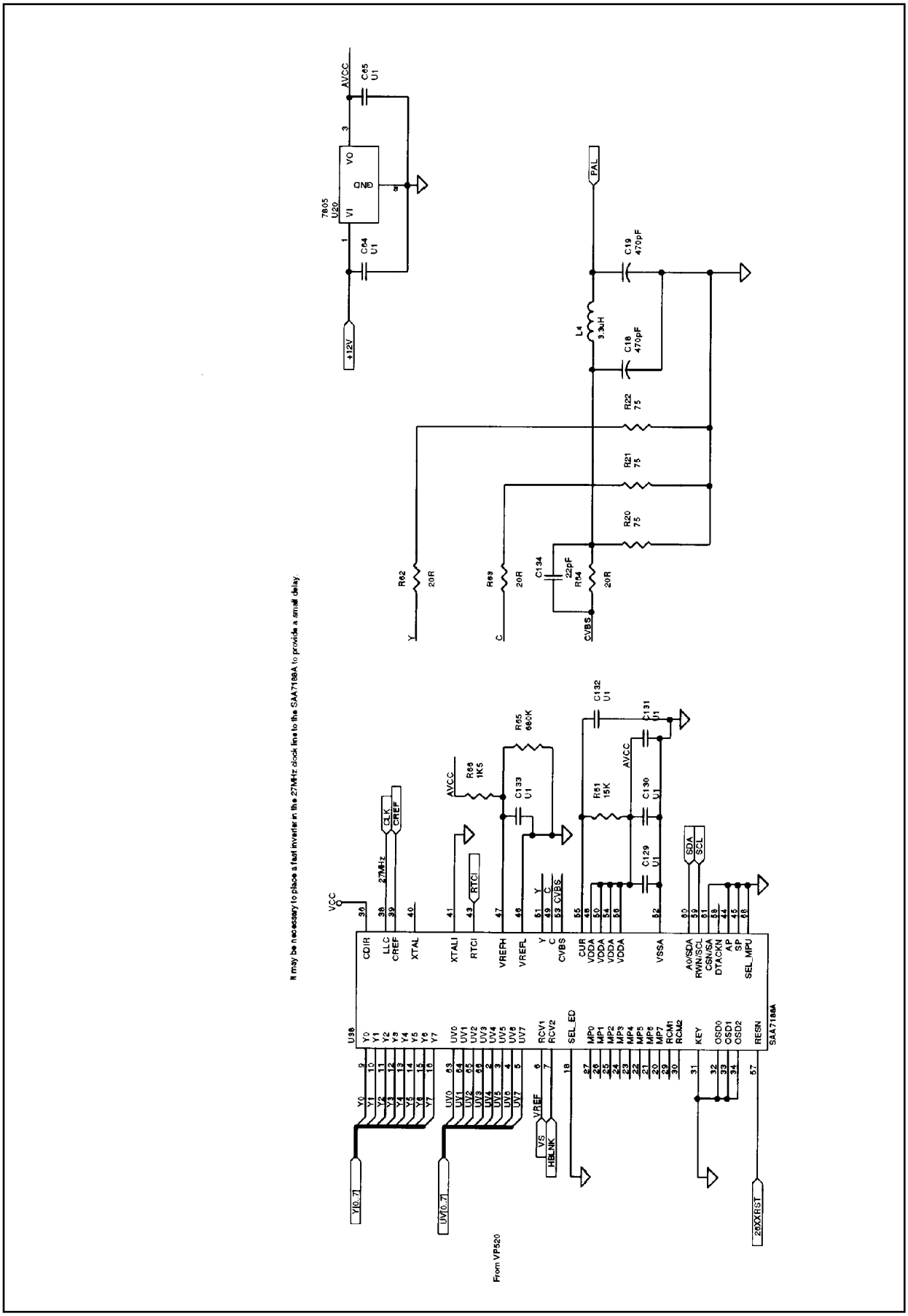
7805
U20
VI
GND
VO
+12V
AVCC
C64 U1
C65 U1
C19 470pF
C18 470pF
L4 3.3uH
PAL
R22 75
R21 75
R20 75
R62 20R
R63 20R
R64 20R
C134 22pF
CVBS
Y
C
R65 66K
R69 1K5
R61 15K
C132 U1
C131 U1
C130 U1
C129 U1
C133 U1
CLK
CREF
27MHz
RTCI
SDA
SCL
VCC
U38
CDIR
LLC
CREF
XTAL
XTALI
RTCI
VREFH
VREFL
Y
C
CVBS
CUR
VDDA
VSSA
A0/SDA
RWN/SCL
CSN/SA
DTACKN
AP
SP
SEL_MPU
SEL_ED
RCV1
RCV2
KEY
OSD0
OSD1
OSD2
RESN
SAA7188A
Y0..7
UV0..7
VREF
VS
HBLNK
26XXRST
From VP520
It may be necessary to place a fast inverter in the 27MHz clock line to the SAA7188A to provide a small delay.

Fig.2

COMPOSITE VIDEO INTERFACING FOR THE VP520S

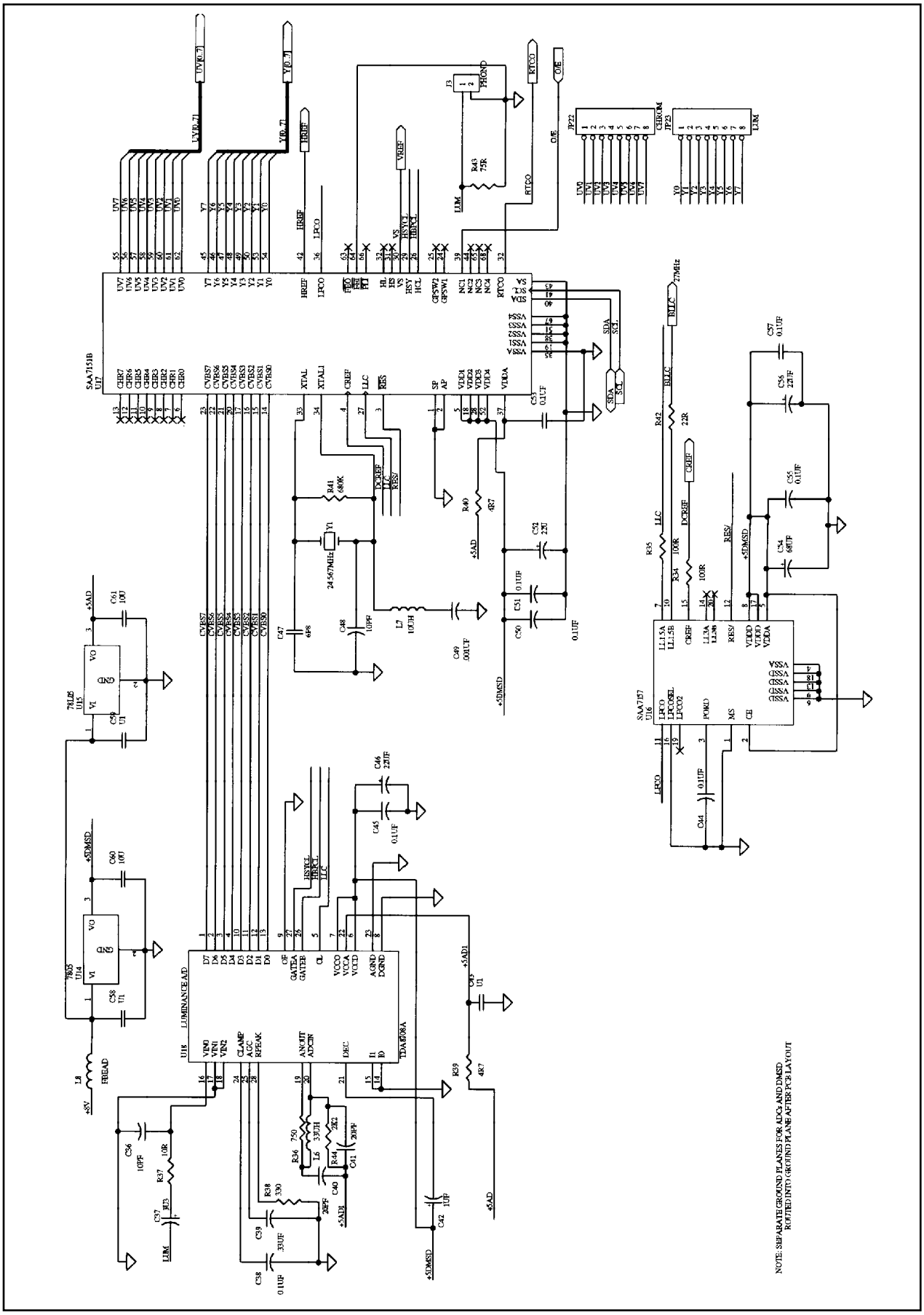

Fig.3

COMPOSITE VIDEO INTERFACING FOR THE VP520S

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